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Response Dated 9/16/2005
Supplemental Response to Office action dated 7/25/2005

 Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A system ~~comprising:~~

~~system~~ to test whether a device under test conforms to a physical layer

communications standard, the ~~testing~~ system comprising:

a plurality of lane cards to transmit data on a plurality of data lanes to the

device under test according to a test pattern and according to the physical layer

communications standard;

a deskew card to prepare deskew information according to the test pattern

and independent of the lane cards according to the physical layer communications

~~standard;~~ standard, the deskew card to evaluate incoming deskew information

included with received incoming data independent of the lane cards according to

the physical layer communications standard

~~a computer coupled to the testing system~~

wherein the system generates arbitrarily long test data on the data lanes

according to the test pattern.

Claim 2 (Previously presented): The system of claim 1 wherein the test pattern is arbitrarily long.

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Claim 3 (Previously presented): The system of claim 1 wherein the deskew card is further to generate the test pattern independent of the data lanes.

Claim 4 (Previously presented): The system of claim 1 wherein the number of data lanes is 16 and the physical layer communications standard is the Serdes Framer Interface Level 5 (SFI-5) standard.

Claim 5 (Original): The system of claim 1 wherein the lane cards each transmit data on two data lanes.

Claim 6 (Original): The system of claim 1 wherein the lane cards each include two lane Field Programmable Gate Arrays.

Claim 7 (Currently Amended): The system of claim 1 ~~wherein the~~ coupled to a computer that includes software which when executed provides a management user interface that allows a user to access the system.

Claim 8 (Currently amended): A testing system to test whether a system under test conforms to a physical layer communications standard, the testing system comprising:

      a plurality of lane cards to transmit data on a plurality of data lanes to the system under test according to a test pattern and according to the physical layer communications standard, and to receive data on the plurality of data lanes from the system under test;

      a deskew card to prepare outgoing deskew information for outgoing data independent of the lane cards according to the test pattern and according to the physical

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layer communications standard, and to evaluate incoming deskew information included

with received incoming data independent of the lane cards according to the physical layer

communications standard

wherein the system generates arbitrarily long test data on the data lanes according

to the test pattern.

Claim 9 (Canceled)

Claim 10 (Previously presented): The testing system of claim 8 wherein the testing system generates

test data according to the test pattern on each of the data lanes independent of the other data lanes.

Claim 11(Previously presented): The testing system of claim 8 wherein the number of data lanes is

16, and the physical layer communications standard is the Serdes Framer Interface Level 5 (SFI-5)

standard.

Claim 12 (Original): The testing system of claim 8 wherein each lane card transmits data on two

data lanes.

Claim 13 (Original): The testing system of claim 8 wherein each of the lane cards include two lane

Field Programmable Gate Arrays.

Claim 14 (Original): The testing system of claim 8 having a computer coupled thereto.

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Claim 15 (Original): The testing system of claim 14 wherein the computer includes software which when executed provides a management user interface that allows a user to monitor and control the testing system.

Claim 16 (Previously presented): A method for transmitting test data according to a physical layer communications standard comprising:

starting a lane counter;

selecting a selected test pattern based on the lane counter;

selecting a pattern seed based on the selecting and the lane counter;

generating a current generated test pattern based on the pattern seed and the selected test seed;

transmitting the current generated test pattern;

generating a next generated test pattern based on the selected test pattern and the current generated pattern;

storing the next generated test pattern.

Claim 17 (Previously presented): The method of claim 16 further comprising:

incrementing the lane counter;

selecting the selected test pattern based on the lane counter;

preparing the pattern seed based on the selected test pattern;

generating the current generated pattern based on the selected test pattern and the next generated test pattern;

evaluating whether to transmit the current generated pattern or a header based on the lane, the evaluating based on the lane counter;

transmitting either the current generated pattern or the header based on the evaluating.

Claim 18 (Original): The method of claim 17 wherein the evaluating comprises selecting the header when a value of the lane counter corresponds to a deskew lane, and selecting the current generated pattern when a value of the lane counter corresponds to a data lane.

Claim 19 (Previously presented): A method for receiving test data according to a physical layer communications standard comprising:

starting a lane counter;

receiving incoming data;

synchronizing the incoming data;

selecting a test pattern based on a value of the lane counter;

evaluating whether to use the incoming data or a stored next generated pattern to generate an anticipated pattern;

generating an anticipated pattern based on the evaluating and the test pattern;

comparing the generated anticipated pattern with the incoming data;

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.flagging an error condition if the generated anticipated pattern and the incoming

data do match based on the comparing.

Claim 20 (Previously presented): The method of claim 19 further comprising:

generating the next pattern based on the test pattern and the anticipated generated

pattern;

storing the next generated pattern as a stored next generated pattern;

incrementing the lane counter;

Claim 21 (Previously presented): A transmitter circuit to transmit deskew data conforming to a

physical layer communications standard, the transmitter circuit comprising:

a lane counter coupled to a pattern select unit a pattern seed unit, and a current

pattern unit, the lane counter to provide a lane value from 0 to 16 and to increment the

lane value;

the pattern select unit to select a pattern based on the lane value and to provide a

selected pattern to the pattern seed unit, a current pattern generation unit and a next

pattern generation unit;

the current pattern unit to store a next generated pattern generated by the next

pattern generation unit as a stored current pattern, and to receive the lane value from the

lane counter;

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the pattern seed unit to provide a pattern seed to a first mux based on the selected

pattern and the lane value;

the first mux to select between the pattern seed received from the pattern seed unit

and the stored current pattern received from the current pattern unit, and to provide input

to the current pattern generation unit;

the current pattern unit to generate a current generated pattern based on input

received from the first mux and the selected pattern;

the next pattern generation unit to generate the next generated pattern based on the

current generated pattern and the selected pattern;

a second mux to select between transmitting a header or the current generated

pattern based on the lane value.

Claim 22 (Previously presented): A receiver circuit to receive deskew data transmitted according to

a physical layer communications standard, the receiver circuit comprising:

a receive line to receive incoming data, the receive line coupled to a frame

synchronization unit and a compare unit;

the frame synchronization unit to identify a data location in the incoming data,

and to provide the data location to a lane counter and a pattern state machine;

the a lane counter to provide a lane value in the range from 0 to 16 and to

increment the lane value, the lane counter to provide the lane value to a pattern select

unit, a current pattern unit, and the pattern state machine;

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the pattern select unit to select a selected pattern based on the lane value and to provide the selected pattern to an anticipated pattern generation unit and a next pattern generation unit;

the current pattern unit to receive a next generated pattern from the next pattern generation unit and store the next generated pattern as a current pattern, the current pattern unit to provide the current pattern to a mux based on the lane value;

the mux to select between the current pattern and the incoming data based on a an output from the pattern state machine, and to provide either the current pattern or the incoming data to the anticipated pattern generation unit as a mux selection;

the anticipated pattern generation unit to receive the mux selection from the mux and to generate an anticipated generated pattern based on the mux selection;

the compare unit to evaluate whether the incoming data corresponds to the anticipated generated pattern, and to provide a result and the incoming data to the pattern state machine.